

10 Rec'd Patent 28 FEB 2002

FORM PTO-1390 (REV. 9-2001)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY'S DOCKET NUMBER 085909-000000US
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371			U.S. APPLICATION NO. (If known, see 37 CFR 1.5) unassigned 10/070280
INTERNATIONAL APPLICATION NO. PCT/CA00/00996	INTERNATIONAL FILING DATE 01 September 2000 (01.09.2000)	PRIORITY DATE CLAIMED 01 September 1999 (01.09.1999)	
TITLE OF INVENTION IMPROVED METHOD AND APPARATUS FOR UP- AND DOWN-CONVERSION OF RADIO FREQUENCY (RF) SIGNALS			
APPLICANT(S) FOR DO/EO/US MANKU, Tajinder, et al.			
Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:			
<ol style="list-style-type: none"> 1. <input checked="" type="checkbox"/> This is a FIRST submission of items concerning a filing under 35 U.S.C. 371. 2. <input type="checkbox"/> This is a SECOND or SUBSEQUENT submission of items concerning a filing under 36 U.S.C. 371. 3. <input checked="" type="checkbox"/> This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below. 4. <input checked="" type="checkbox"/> The US has been elected by the expiration of 19 months from the priority date (Article 31). 5. <input checked="" type="checkbox"/> A copy of the International Application as filed (35 U.S.C. 37(c)(2)) <ol style="list-style-type: none"> a. <input checked="" type="checkbox"/> is attached hereto (required only if not communicated by the International Bureau). b. <input type="checkbox"/> has been communicated by the International Bureau c. <input type="checkbox"/> is not required, as the application was filed in the United States Receiving Office (RO/US). 6. <input type="checkbox"/> An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)). <ol style="list-style-type: none"> a. <input type="checkbox"/> is attached hereto. b. <input type="checkbox"/> has been previously submitted under 35 U.S.C. 154(d)(4). 7. <input checked="" type="checkbox"/> Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)). <ol style="list-style-type: none"> a. <input type="checkbox"/> are attached hereto (required only if not communicated by the International Bureau). b. <input type="checkbox"/> have been communicated by the International Bureau. c. <input type="checkbox"/> have not been made; however, the time limit for making such amendments has NOT expired. d. <input checked="" type="checkbox"/> have not been made and will not be made. 8. <input type="checkbox"/> An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)). 9. <input type="checkbox"/> An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)). 10. <input type="checkbox"/> An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)). 			
Items 11 to 20 below concern document(s) or information included:			
<ol style="list-style-type: none"> 11. <input type="checkbox"/> An Information Disclosure Statement under 37 CFR 1.97 and 1.98. 12. <input type="checkbox"/> An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included. 13. <input checked="" type="checkbox"/> A FIRST preliminary amendment. 14. <input type="checkbox"/> A SECOND or SUBSEQUENT preliminary amendment. 15. <input type="checkbox"/> A substitute specification. 16. <input type="checkbox"/> A change of power of attorney and/or address letter. 17. <input type="checkbox"/> A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 – 1.825. 18. <input type="checkbox"/> A second copy of the published international application under 36 U.S.C. 19. <input type="checkbox"/> A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4). 20. <input checked="" type="checkbox"/> Other items or information: <ol style="list-style-type: none"> a. Express Mail Label No. EL585155667US mailed on February 28, 2002 b. Return Postcard c. International Publication No. WO 01/17122 A1 d. International Preliminary Examination Report e. Written Opinion f. Response to Written Opinion 			

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I/S/ Application no. known, see 37 CFR 1.51 unassigned 107070280		INTERNATIONAL APPLICATION NO. PCT/CA00/00996		ATTORNEY'S DOCKET NUMBER 085909-000000US	
21. <input checked="" type="checkbox"/> The following fees are submitted:				CALCULATIONS PTO USE ONLY	
BASIC NATIONAL FEE (37 CFR 1.492(A) (1) – (5)): Neither international preliminary examination fee (37 CFR 1.492) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO \$1040.00 International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search report prepared by the EPO of JPO \$890.00 International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO \$740.00 International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) \$710.00 International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)(4) \$100.00					
ENTER APPROPRIATE BASIC FEE AMOUNT =				\$890.00	
Surcharge of \$130.00 for furnishing the oath or declaration later than <input type="checkbox"/> 20 <input type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492(e)).				\$0	
CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	\$	
Total claims	31 - 20 =	11	x \$18.00	\$198.00	
Independent claims	1-3 =	0	x \$84.00	\$0	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ 280.00	\$0	
TOTAL OF ABOVE CALCULATIONS =				\$198.00	
<input type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.				\$0	
SUBTOTAL =				\$1088.00	
Processing fee of \$130.00 for furnishing the English translation later than <input type="checkbox"/> 20 <input type="checkbox"/> 30 months from the earliest claimed priority date (37 CFT 1.492(f)).				\$0	
TOTAL NATIONAL FEE =				\$1088.00	
Fee for recording the enclosed assignment (37 CFR 1.2(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). \$40.00 per property +				\$0	
TOTAL FEES ENCLOSED =				\$1088.00	
				Amount to be refunded:	\$0
				charged:	\$1088.00
a. <input type="checkbox"/> A check in the amount of \$_____ to cover the above fees is enclosed. b. <input checked="" type="checkbox"/> Please charge my Deposit Account No. <u>20-1430</u> in the amount of \$1088.00 to cover the above fees. c. <input checked="" type="checkbox"/> The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. <u>20-1430</u> . A duplicate copy of this sheet is enclosed. d. <input type="checkbox"/> Fees are to be charged to a credit card. WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.					
NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b) must be filed and granted to restore the application to pending status.					
SEND ALL CORRESPONDENCE TO: Townsend and Townsend and Crew LLP 2 Embarcadero Center, 8 th Floor San Francisco, CA 94111			<div style="display: flex; align-items: center;"> <div style="flex: 1;"> </div> <div style="flex: 1; text-align: right;"> February 28, 2002 </div> </div> <div style="display: flex; justify-content: space-between; margin-top: 5px;"> SIGNATURE DATE </div> <div style="display: flex; justify-content: space-between; margin-top: 10px;"> Kenneth R. Allen </div> <div style="display: flex; justify-content: space-between; margin-top: 5px;"> NAME </div> <div style="display: flex; justify-content: space-between; margin-top: 10px;"> 27,301 </div> <div style="display: flex; justify-content: space-between; margin-top: 5px;"> REGISTRATION NUMBER </div>		

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PATENT

Attorney Docket No. 085909-000000US

Client Reference No. 08887955US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

MANKU, Tajinder et al.

Application No.: Not yet assigned

Filed: Herewith

For: IMPROVED METHOD AND
APPARATUS FOR UP-AND-DOWN-
CONVERSION OF RADIO
FREQUENCY (RF) SIGNALS

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to the examination of the above-referenced application, please enter the following amendments.

IN THE CLAIMS:

Applicants respectfully submit herewith previous amendments to the claims that were made pursuant Article 34 in response to the Written Opinion during the International Phase and at this time, Applicants have deleted claims 31 and 32 and have reformatted the previously added claim 33 in accordance with preferred U.S. patent practice. Applicants have also amended claims 25, 26, 27, 28 and 30 to eliminate multiple dependencies.

Respectfully submitted,

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WHAT IS CLAIMED IS:

1. A synthesizer for generating signals to be input to successive mixers for modulating or demodulating an input signal $x(t)$, said synthesizer comprising:
a first signal generator for producing a first mixing signal ϕ_1 which varies irregularly over time; and
a second signal generator for producing a second mixing signal ϕ_2 which varies irregularly over time;
where $\phi_1 * \phi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither ϕ_1 nor ϕ_2 has significant power at the frequency of said local oscillator signal being emulated.
2. The synthesizer of claim 1, wherein signals used to generate ϕ_1 and ϕ_2 do not have a significant amount of power at the output frequency of said output signal $x(t)$ ϕ_1 ϕ_2 .
3. The synthesizer of claim 2, wherein $\phi_1 * \phi_1 * \phi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)$ ϕ_1 ϕ_2 .
4. The synthesizer of claim 3, wherein $\phi_2 * \phi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)$ ϕ_1 ϕ_2 .
5. The synthesizer of claim 4, wherein said first and second mixing signals ϕ_1 and ϕ_2 are generating using a single time base.
6. The synthesizer of claim 4, wherein said first and second mixing signals ϕ_1 and ϕ_2 are digital waveforms.
7. The synthesizer of claim 4, wherein said first and second mixing signals ϕ_1 and ϕ_2 are square waveforms.
8. The synthesizer of claim 4, wherein said first and second mixing signals ϕ_1 and ϕ_2 are randomly generated.
9. The synthesizer of claim 4, wherein said first and second mixing signals ϕ_1 and ϕ_2 are pseudo-randomly generated.

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10. The synthesizer of claim 4, wherein said first and second mixing signals ϕ_1 and ϕ_2 are periodic functions of time.
11. The synthesizer of claim 4, wherein said first and second signal generators comprise:
pulse removal means for removing pulses from a local oscillator signal which has a frequency of twice the RF carrier, generating said first mixing signal ϕ_1 ; and
complementary means for generating said second mixing signal ϕ_2 .
12. The synthesizer of claim 4, wherein said pulse removal means comprises:
a pulse swallower for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and swallowing each pulse with a control signal S; and
a divide by two circuit for receiving and dividing said pulse swallowed signal by two, producing said first mixing signal ϕ_1 .
13. The synthesizer of claim 12, wherein said complementary means comprises:
a delay circuit for receiving and delaying said control signal S to be synchronized in time with said first mixing signal ϕ_1 , outputting said delayed control signal S as said second mixing signal ϕ_2 .
14. The synthesizer of claim 4, wherein said first and second signal generators comprise:
shift register means for generating said first and second mixing signals ϕ_1 and ϕ_2 by shifting out corresponding predetermined sequences.
15. The synthesizer of claim 14, wherein said shift register means comprises:
a shift register for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said first mixing signal ϕ_1 , by shifting out a predetermined sequence.
16. The synthesizer of claim 15, wherein said second signal generator comprises:
an exclusive-OR (XOR) circuit for comparing outputs of consecutive latches in said shift register; and

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a second shift register being clocked by said XOR output, and generating said second mixing signal ϕ_2 , by shifting out a second predetermined sequence.

17. The synthesizer of claim 15, wherein said second signal generator comprises:

a third shift register for receiving said oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said second mixing signal ϕ_2 , by shifting out a predetermined sequence.

18. The synthesizer of claim 4, wherein said first and second signal generators comprise:

means for generating said first mixing signal ϕ_1 from an oscillator signal at the frequency of the local oscillator signal being emulated, and a control signal S having edges aligned with said oscillator signal; and

means for delaying said control signal S to produce said second mixing signal ϕ_2 .

19. The synthesizer of claim 18, wherein said means for delaying comprises:
a delay latch for sampling said control signal S at the frequency of the local oscillator signal being emulated; and

an inverter for receiving and inverting said delay latched control signal S to produce said second mixing signal ϕ_2 .

20. The synthesizer of claim 19, wherein said means for generating said first mixing signal ϕ_1 comprises:

a second inverter for receiving the oscillator signal at the frequency of the local oscillator signal being emulated; and

an exclusive-OR (XOR) circuit for comparing said inverted oscillator signal with said latched input signal $x(t)$, producing said first mixing signal ϕ_1 .

21. The synthesizer of claim 4, wherein said first signal generator comprises:
a shift register with a feedback loop.

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22. The synthesizer of claim 21, wherein said first signal generator comprises:
a shift register for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said first mixing signal ϕ_1 , by shifting out a predetermined sequence; and
a modulo-2 multiplier for receiving said first mixing signal ϕ_1 and the output of an earlier latch in said shift register, feeding an output into a later latch in said shift register.
23. The synthesizer of claim 4 comprising:
one or more additional signal generators for producing one or more additional mixing signals, varying irregularly over time;
where the product of all of said mixing signals has significant power at the frequency of a local oscillator signal being emulated, and none of said all of said mixing signals has significant power at the frequency of said local oscillator signal being emulated.
24. The synthesizer of claim 4, where said first signal generator comprises:
a divide by 2 circuit for receiving an oscillator signal at the frequency of the local oscillator signal being emulated; and
a divide by 4 circuit for receiving said oscillator signal at the frequency of the local oscillator signal being emulated;
selector means for routing either the output of said divide by 2 circuit or said divide by 4 circuit to an output, said output producing said first mixing signal ϕ_1 .
25. The synthesizer of claim 12, wherein said control signal S comprises a random signal.
26. The synthesizer of claim 12, wherein said control signal S comprises a pseudo-random signal.
27. The synthesizer of claim 12, wherein said control signal S comprises a periodic signal.
28. The synthesizer of claim 12, comprising:
a delta-sigma (Δ -S) modulator for generating said control signal S .

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29. The synthesizer of claim 4 comprising:
first and second latches which are clocked via a common clock, to align said first and
second mixing signals ϕ_1 and ϕ_2 .
30. An integrated circuit comprising the synthesizer of claim 1.
31. The synthesizer of claim 4, wherein the patterns of said first and second mixing
signals ϕ_1 and ϕ_2 are different from one another.

COMPARE DOCUMENT

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WHAT IS CLAIMED IS:

1. A synthesizer for generating signals to be input to successive mixers for modulating or demodulating an input signal $x(t)$, said synthesizer comprising:
a first signal generator for producing a first ~~time-varying~~mixing signal ϕ_1 , which varies irregularly over time; and
a second signal generator for producing a second ~~time-varying~~mixing signal ϕ_2 , which varies irregularly over time;
where $\phi_1 * \phi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither ϕ_1 nor ϕ_2 has significant power at the frequency of said local oscillator signal being emulated.
2. The synthesizer of claim 1, wherein signals used to generate ϕ_1 and ϕ_2 do not have a significant amount of power at the output frequency of said output signal $x(t)$ $\phi_1 \phi_2$.
3. The synthesizer of claim 2, wherein $\phi_1 * \phi_1 * \phi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)$ $\phi_1 \phi_2$.
4. The synthesizer of claim 3, wherein $\phi_2 * \phi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)$ $\phi_1 \phi_2$.
5. The synthesizer of claim 4, wherein said first and second ~~time-varying~~mixing signals ϕ_1 and ϕ_2 are irregulargenerating using a single time base.
6. The synthesizer of claim 4, wherein said first and second ~~time-varying~~mixing signals ϕ_1 and ϕ_2 are digital waveforms.
7. The synthesizer of claim 4, wherein said first and second ~~time-varying~~mixing signals ϕ_1 and ϕ_2 are square waveforms.
8. The synthesizer of claim 4, wherein said first and second ~~time-varying~~mixing signals ϕ_1 and ϕ_2 are randomly generated.
9. The synthesizer of claim 4, wherein said first and second ~~time-varying~~mixing signals ϕ_1 and ϕ_2 are pseudo-randomly generated.

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10. The synthesizer of claim 4, wherein said first and second ~~time-varying~~mixing signals ϕ_1 and ϕ_2 are periodic functions of time.
11. The synthesizer of claim 4, wherein said first and second signal generators comprise:
pulse removal means for removing pulses from a local oscillator signal which has a frequency of twice the RF carrier, generating said first ~~time-varying~~mixing signal ϕ_1 ; and
complementary means for generating said second ~~time-varying~~mixing signal ϕ_2 .
12. The synthesizer of claim 4, wherein said pulse removal means comprises:
a pulse swallower for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and swallowing each pulse with a control signal S; and
a divide by two circuit for receiving and dividing said pulse swallowed signal by two, producing said first ~~time-varying~~mixing signal ϕ_1 .
13. The synthesizer of claim 12, wherein said complementary means comprises:
a delay circuit for receiving and delaying said control signal S to be synchronized in time with said first ~~time-varying~~mixing signal ϕ_1 , outputting said delayed control signal S as said second ~~time-varying~~mixing signal ϕ_2 .
14. The synthesizer of claim 4, wherein said first and second signal generators comprise:
shift register means for generating said first and second ~~time-varying~~mixing signals ϕ_1 and ϕ_2 by shifting out corresponding predetermined sequences.
15. The synthesizer of claim 14, wherein said shift register means comprises:
a shift register for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said first ~~time-varying~~mixing signal ϕ_1 , by shifting out a predetermined sequence.
16. The synthesizer of claim 15, wherein said second signal generator comprises:

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an exclusive-OR (XOR) circuit for comparing outputs of consecutive latches in said shift register; and
a second shift register being clocked by said XOR output, and generating said second ~~time-varying~~mixing signal ϕ_2 , by shifting out a second predetermined sequence.

17. The synthesizer of claim 15, wherein said second signal generator comprises:

a third shift register for receiving said oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said second ~~time-varying~~mixing signal ϕ_2 , by shifting out a predetermined sequence.

18. The synthesizer of claim 4, wherein said first and second signal generators comprise:

means for generating said first ~~time-varying~~mixing signal ϕ_1 from an oscillator signal at the frequency of the local oscillator signal being emulated, and a control signal S having edges aligned with said oscillator signal; and
means for delaying said control signal S to produce said second ~~time-varying~~mixing signal ϕ_2 .

19. The synthesizer of claim 18, wherein said means for delaying comprises:
a delay latch for sampling said control signal S at the frequency of the local oscillator signal being emulated; and

an inverter for receiving and inverting said delay latched control signal S to produce said second ~~time-varying~~mixing signal ϕ_2 .

20. The synthesizer of claim 19, wherein said means for generating said first ~~time-varying~~mixing signal ϕ_1 comprises:

a second inverter for receiving the oscillator signal at the frequency of the local oscillator signal being emulated; and

an exclusive-OR (XOR) circuit for comparing said inverted oscillator signal with said latched input signal $x(t)$, producing said first ~~time-varying~~mixing signal ϕ_1 .

21. The synthesizer of claim 4, wherein said first signal generator comprises:
a shift register with a feedback loop.

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22. The synthesizer of claim 21, wherein said first signal generator comprises:
a shift register for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said first time-varying mixing signal ϕ_1 , by shifting out a predetermined sequence; and
a modulo-2 multiplier for receiving said first time-varying mixing signal ϕ_1 and the output of an earlier latch in said shift register, feeding an output into a later latch in said shift register.
23. The synthesizer of claim 4 comprising:
one or more additional signal generators for producing one or more additional time-varying mixing signals, varying irregularly over time;
where the product of all of said time-varying mixing signals has significant power at the frequency of a local oscillator signal being emulated, and none of said all of said time-varying mixing signals has significant power at the frequency of said local oscillator signal being emulated.
24. The synthesizer of claim 4, where said first signal generator comprises:
a divide by 2 circuit for receiving an oscillator signal at the frequency of the local oscillator signal being emulated; and
a divide by 4 circuit for receiving said oscillator signal at the frequency of the local oscillator signal being emulated;
selector means for routing either the output of said divide by 2 circuit or said divide by 4 circuit to an output, said output producing said first time-varying mixing signal ϕ_1 .
25. The synthesizer ~~of any one of claims 12, 13, 18, 19 or 240~~, wherein said control signal S comprises a random signal.
26. The synthesizer ~~of any one of claims 12, 13, 18, 19 or 240~~, wherein said control signal S comprises a pseudo-random signal.
27. The synthesizer ~~of any one of claims 12, 13, 18, 19 or 240~~, wherein said control signal S comprises a periodic signal.
28. The synthesizer ~~of any one of claims 12, 13, 18, 19 or 240~~, comprising:

a delta-sigma (i.e., Δ -S) modulator for generating said control signal S.

29. The synthesizer of claim 4 comprising:

first and second latches which are clocked via a common clock, to align said first and second ~~time-varying~~ mixing signals ϕ_1 and ϕ_2 .

30. An integrated circuit comprising the synthesizer of ~~any one of claims 1-29~~ claim 1.

~~31. A computer readable memory medium, storing computer software code in a hardware development language for fabrication of an integrated circuit comprising the synthesizer of any one of claims 1-29.~~

~~32. A computer data signal embodied in a output wave, said computer data signal comprising computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio transmitter of any one of claims 1-29.~~

33. The synthesizer of claim 4, wherein the patterns of said first and second mixing signals ϕ_1 and ϕ_2 are different from one another.

**Improved Method and Apparatus for Up- and Down- Conversion of Radio
Frequency (RF) Signals**

5 The present invention relates generally to communications, and more specifically, to a fully-integrable method and apparatus for up- and down-conversion of radio frequency (RF) and baseband signals with improved performance.

Background of the Invention

10 Many communication systems modulate electromagnetic signals from baseband to higher frequencies for transmission, and subsequently demodulate those high frequencies back to their original frequency band when they reach the receiver. The original (or baseband) signal, may be, for example: data, voice or video. These baseband signals may be produced by transducers such as microphones or video cameras, be computer generated, or transferred from an
15 electronic storage device. In general, the high transmission frequencies provide longer range and higher capacity channels than baseband signals, and because high frequency RF signals can propagate through the air, they can be used for wireless channels as well as hard wired or fibre channels.

20 All of these signals are generally referred to as radio frequency (RF) signals, which are electromagnetic signals, that is, waveforms with electrical and magnetic properties within the electromagnetic spectrum normally associated with radio wave propagation. The electromagnetic spectrum was traditionally divided into 26 alphabetically designated bands, however, the International Telecommunication Union (ITU) formally recognizes 12 bands, from 30 Hz to 3000 GHz. New bands,
25 from 3 THz to 3000 THz, are under active consideration for recognition.

Wired communication systems which employ such modulation and demodulation techniques include computer communication systems such as local area networks (LANs), point to point signalling, and wide area networks (WANs) such as the Internet. These networks generally communication data signals over
30 electrical or optical fibre channels. Wireless communication systems which may employ modulation and demodulation include those for public broadcasting such as AM and FM radio, and UHF and VHF television. Private communication systems may include cellular telephone networks, personal paging devices, HF radio systems used by taxi services, microwave backbone networks, interconnected appliances
35 under the Bluetooth standard, and satellite communications. Other wired and

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wireless systems which use RF modulation and demodulation would be known to those skilled in the art.

One of the current problems in the art, is to develop physically small and inexpensive modulation and demodulation techniques and devices that have good performance characteristics. For cellular telephones, for example, it is desirable to have transmitters and receivers (which may be referred to in combination as a transceiver) which can be fully integrated onto integrated circuits (ICs).

Several attempts at completely integrated transceiver designs have met with limited success. For example, most RF topology typically requires at least two high quality filters that cannot be economically integrated within any modern IC technology. Other RF receiver topologies exist, such as image rejection architectures, which can be completely integrated on a chip, but lack in overall performance. Most receivers use the "super-heterodyne" topology, which provides excellent performance, but does not meet the desired level of integration for modern wireless systems.

Existing transceiver solutions and their associated problems and limitations are summarized below.

1. Super-heterodyne:

The super-heterodyne receiver uses a two-step frequency translation method to convert an RF signal to a baseband signal. **Figure 1** presents a block diagram of a typical super-heterodyne receiver **10**. Generally, the mixers labelled **M1 12**, **MI 14**, and **MQ 16** are used to translate an incoming RF signal to baseband or to some intermediate frequency (IF). The balance of the components amplify the signal being processed and filter noise from it.

More specifically, the RF band pass filter (BPF1) **18** first filters the incoming signal and corruptive noise coming from the antenna **20**, attenuating out of band signals and passing the desired signal (note that this band pass filter **18** may also be a duplexer). A low noise amplifier **22** then amplifies the filtered antenna signal, increasing the strength of the RF signal and reducing the noise figure of the receiver **10**. The signal is next filtered by another band pass filter (BPF2) **24** usually identified as an image rejection filter. The desired signal, plus residual unwanted signals, then enter mixer **M1 12** which multiplies this signal with a periodic sinusoidal signal generated by the local oscillator (LO1) **26**. The mixer **M1 12** receives the signal from the image rejection filter **24** and causes both a down-conversion and an up-

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conversion in the frequency domain. Usually, the down-converted portion is retained at the so-called "Intermediate Frequency" (IF).

Generally, a mixer is a circuit or device that accepts as its input two different frequencies and presents at its output:

- 5 (a) a signal equal in frequency to the sum of the frequencies of the input signals;
- (b) a signal equal in frequency to the difference between the frequencies of the input signals; and
- (c) the original input frequencies.

Note that the frequency conversion process causes a second band of
10 frequencies to be superimposed upon the desired signal at the IF frequency. These "image frequencies" are also passed by the band pass filter 24 and corrupt the desired signal. Note also that the typical embodiment of a mixer is a digital switch, which may generate significantly more tones than those described in (a) through (c).

The IF signal is next filtered by a band pass filter (BPF3) 28 typically called
15 the channel filter, which is centred around the IF frequency, thus filtering out mixer signals (a) and (c) above.

The signal is then amplified by an amplifier (IFA) 30, and is split into its in-phase (I) and quadrature (Q) components, using mixers MI 14 and MQ 16, and orthogonal mixing signals generated by local oscillator (LO2) 32 and 90 degree
20 phase shifter 34. LO2 32 generates a regular, periodic signal which is typically tuned to the IF frequency, so that the signals coming from the outputs of MI 14 and MQ 16 are now at baseband, that is, the frequency at which they were originally generated. The two signals are next filtered using low pass filters LPFI 36 and LPFQ 38 to remove the unwanted products of the mixing process, producing baseband I and Q
25 signals. The signals may then be amplified by gain-controlled amplifiers AGCI 40 and AGCQ 42, and digitized via analog to digital converters ADI 44 and ADQ 46 if required by the receiver.

The main problems with the super-heterodyne design are:

- 30 • it requires expensive off-chip components, particularly band pass filters 18, 24, 28, and low pass filters 36, 38 to remove unwanted signal components;
- the off-chip components require design trade-offs that increase power consumption and reduce system gain;
- image rejection is limited by the off-chip components, not by the target integration technology;
- 35 • isolation from digital noise can be a problem; and

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- it is not fully integratable.

2. Image Rejection Architectures:

Several image rejection architectures exist, but are not widely used. The two most well known being the Hartley Image Rejection Architecture and the Weaver Image Rejection Architecture. There are other designs, which are generally based on these two architectures, and other methods which employ poly-phase filters to cancel image components. Generally, either accurate signal phase shifts or accurate generation of quadrature local oscillators are employed in these architectures to cancel the image frequencies. The amount of image cancellation is directly dependent upon the degree of accuracy in producing the phase shift or in producing the quadrature local oscillator signals.

Although the integratability of these architectures is high, their performance is relatively poor due to the required accuracy of the phase shifts and quadrature oscillators. This architecture has been used for dual mode receivers on a single chip.

3. Direct Conversion:

Direct conversion architectures demodulate RF signals to baseband in a single step, by mixing the RF signal with a local oscillator signal at the carrier frequency of the RF signal. There is therefore no image frequency, and no image components to corrupt the signal. Direct conversion receivers offer a high level of integratability, but also have several important problems. Hence, direct conversion receivers have thus far proved useful only for signalling formats that do not place appreciable signal energy near DC after conversion to baseband.

A typical direct conversion receiver is shown in **Figure 2**. The RF band pass filter (BPF1) 18 first filters the signal coming from the antenna 20 (this band pass filter 18 may also be a duplexer). A low noise amplifier 22 is then used to amplify the filtered antenna signal, increasing the strength of the RF signal and reducing the noise figure of the receiver 10.

The signal is then split into its quadrature components and demodulated in a single stage using mixers M1 14 and MQ 16, and orthogonal signals generated by local oscillator (LO2) 32 and 90 degree phase shifter 34. LO2 32 generates a regular, periodic signal which is tuned to the incoming wanted frequency rather than an IF frequency as in the case of the super-heterodyne receiver. The signals coming from the outputs of M1 14 and MQ 16 are now at baseband, that is, the frequency at which they were originally generated. The two signals are next filtered

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using low pass filters LPFI 36 and LPFQ 38, are amplified by gain-controlled amplifiers AGCI 40 and AGCQ 42, and are digitized via analog to digital converters ADI 44 and ADQ 46.

Direct conversion RF receivers have several advantages over super-heterodyne systems in term of cost, power, and level of integration, however, there are also several serious problems with direct conversion. These problems include:

- noise near baseband (that is, $1/f$ noise) which corrupts the desired signal;
- local oscillator (LO) leakage in the RF path that creates DC offsets. As the LO frequency is the same as the incoming signal being demodulated, any leakage of the LO signal onto the antenna side of the mixer will pass through to the output side as well;
- local oscillator leakage into the RF path that causes desensitization. Desensitization is the reduction of desired signal gain as a result of receiver reaction to an undesired signal. The gain reduction is generally due to overload of some portion of the receiver, such as the AGC circuitry, resulting in suppression of the desired signal because the receiver will no longer respond linearly to incremental changes in input voltage.
- noise inherent to mixed-signal integrated circuits corrupts the desired signal;
- large on-chip capacitors are required to remove unwanted noise and signal energy near DC, which makes integrability expensive. These capacitors are typically placed between the mixers and the low pass filters; and
- errors are generated in the quadrature signals due to inaccuracies in the 90 degree phase shifter.

4. Near Zero-IF Conversion:

This receiver architecture is similar to the direct conversion architecture, in that the RF input signal band is translated brought close to baseband in a single step using a regular, periodic oscillator signal. However, the desired signal is not brought exactly to baseband and therefore DC offsets and $1/f$ noise do not contaminate the output signal. Image frequencies are again a problem though, as in the case of the super-heterodyne structure.

Additional problems encountered with near zero-IF architectures include:

- the need for very accurate quadrature local oscillators;
- the need for several balanced signal paths for purposes of image cancellation;

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- noise inherent to mixed-signal integrated circuits which corrupts the desired output signal; and
- isolation from digital noise can be a problem.

5. Sub-sampling Down-conversion:

5 This method of signal down-conversion utilizes subsampling of the input signal to effect the frequency translation, that is, the input signal is sampled at a lower rate than the signal frequency. This may be done, for example, by use of a sample and hold circuit.

10 Although the level of integration possible with this technique is the highest among those discussed thus far, the subsampling down-conversion method suffers from two major drawbacks:

- subsampling of the RF signal causes aliasing of unwanted noise power to DC. Sampling by a factor of m increases the down-converted noise power of the sampling circuit by a factor of $2m$; and
- 15 • subsampling also increases the effect of noise in the sampling clock. In fact, the clock phase noise power is increased by m^2 for sampling by a factor of m .

There is therefore a need for a method and apparatus of modulating and demodulating RF signals which allows the desired integrability along with good performance.

20

Summary of the Invention

It is therefore an object of the invention to provide a novel method and system of modulation and demodulation which obviates or mitigates at least one of the disadvantages of the prior art.

25 One aspect of the invention is broadly defined as a first signal generator for producing a first time-varying signal ϕ_1 ; and a second signal generator for producing a second time-varying signal ϕ_2 ; where $\phi_1 * \phi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither ϕ_1 nor ϕ_2 has significant power at the frequency of the local oscillator signal being emulated.

30

Brief Description of the Drawings

These and other features of the invention will become more apparent from the following description in which reference is made to the appended drawings in which:

5 **Figure 1** presents a block diagram of a super-heterodyne system as known in the art;

Figure 2 presents a block diagram of a direct conversion transmitter as known in the art;

10 **Figure 3** presents a mixer and synthesizer arrangement in a broad embodiment of the invention;

Figure 4 (a) presents a first exemplary mixer input signals pairing plotted in amplitude against time, in an embodiment of the invention;

Figure 4 (b) presents a second exemplary mixer input signals pairing plotted in amplitude against time, in an embodiment of the invention;

15 **Figure 5** presents a mixer and synthesizer arrangement for modulation or demodulation of in-phase and quadrature components of an input signal in an embodiment of the invention;

20 **Figure 6** presents a block diagram of an exemplary signal synthesizer in an embodiment of the invention, employing a pulse swallower and a divide-by-2 circuit;

Figure 7 presents a logic diagram of an exemplary signal synthesizer for generating quadrature mixer signals, in an embodiment of the invention;

Figure 8 presents a logic diagram of an exemplary signal synthesizer in an embodiment of the invention, employing a shift register;

25 **Figure 9** presents a logic diagram of an exemplary signal synthesizer in an embodiment of the invention, employing two shift registers;

Figure 10 presents a logic diagram of an exemplary signal synthesizer in an embodiment of the invention, employing an input signal with a frequency equal to the RF carrier;

30 **Figure 11** presents a logic diagram of an exemplary signal synthesizer in an embodiment of the invention, employing a shift register with feedback; and

Figure 12 presents a block diagram of an embodiment of the invention employing N mixers and N time-domain signals.

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Detailed Description of the Invention

The present invention relates to the frequency translation of RF signals to and from baseband in highly integrated receivers and transmitters. It is particularly
5 concerned with the generation of signals used in the translation process which have properties that solve the image-rejection problems associated with heterodyne receivers and transmitters and the LO-leakage and 1/f noise problems associated with direct conversion receivers and transmitters.

A circuit which addresses the objects outlined above, is presented as a block
10 diagram in **Figure 3**. This figure presents a modulator or demodulator topography 70 in which an input signal $x(t)$ is mixed with two synthesized signals (labelled ϕ_1 and ϕ_2) which are irregular and vary in the time domain (TD), to effect the desired modulation or demodulation. The two mixers M1 72 and M2 74 are standard mixers
15 known in the art, having the typical properties of an associated noise figure, linearity response, and conversion gain. The selection and design of these mixers would follow the standards known in the art, and could be, for example, double balanced mixers. Though this figure implies various elements are implemented in analogue form they can be implemented in digital form.

The two synthesizers 76 and 78 generate two time-varying functions ϕ_1 and
20 ϕ_2 that together comprise a virtual local oscillator (VLO) signal. These two functions have the properties that their product emulates a local oscillator (LO) signal that has significant power at the carrier frequency, but neither of the two signals has a significant level of power at the frequency of the LO being emulated. As a result, the desired modulation or demodulation is affected, but there is no LO signal to leak into
25 the RF path.

The representation in **Figure 3** is exemplary, as any two-stage or multiple stage mixing architecture may be used to implement the invention. As well, the synthesizer for generating the time-varying mixer signals ϕ_1 and ϕ_2 may be comprised of a single device, or multiple devices.

In current receiver and transmitter technology, frequency translation of an RF
30 signal to and from baseband is performed by multiplying the input signal by regular, periodic, sinusoids. If one multiplication is performed, the architecture is said to be a direct-conversion or homodyne architecture, while if more than one multiplication is performed the architecture is said to be a heterodyne or super-heterodyne
35 architecture. Direct-conversion transceivers suffer from LO leakage and 1/f noise

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problems which limit their capabilities, while heterodyne transceivers require image-rejection techniques which are difficult to implement on-chip with high levels of performance.

The problems of image-rejection, LO leakage and $1/f$ noise in highly integrated transceivers can be overcome by using more complex signals than simple, regular, periodic, sinusoids in the frequency translation process. These signals have tolerable amounts of power at the RF band frequencies both in the signals themselves and in any other signals produced during their generation. Two example of such signals (ϕ_1 and ϕ_2) are presented in **Figures 4(a) and 4(b)**, and are described in detail hereinafter.

The preferred criteria for selecting the functions ϕ_1 and ϕ_2 are:

- (i) for the signal $x(t)$ to be translated to baseband, $\phi_1(t) * \phi_2(t)$ must have a frequency component at the carrier frequency of $x(t)$;
- (ii) in order to minimize image problems, $\phi_1(t) * \phi_2(t)$ must have less than a tolerable amount energy at frequencies other than the carrier frequency of $x(t)$ or at least far enough away that these image frequencies can be significantly filtered on-chip prior to down-conversion; and
- (iii) in order to minimize LO leakage problems, the signals ϕ_1 and ϕ_2 must not have significant amounts of power in the RF output signal bandwidth. That is, the amount of power generated at the output frequency should not effect the overall system performance of the transmitter or receiver in a significant manner;
- (iv) also to avoid LO leakage found in conventional direct conversion and directly modulated topologies, the signals required to generate ϕ_1 and ϕ_2 or the intermediate signals which occur, should not have a significant amount of power at the output frequency;
- (v) $\phi_2 * \phi_2$ should not have a significant amount of power within the bandwidth of the up-converted RF (output) signal. This ensures that if ϕ_1 leaks into the input port, it does not produce a signal within the RF signal at the output. It also ensures that if ϕ_2 leaks into node between the two mixers, it does not produce a signal within the RF signal at the output; and
- (vi) if $x(t)$ is an RF signal, $\phi_1 * \phi_1 * \phi_2$ should not have a significant amount of power within the bandwidth of the RF signal at baseband. This ensures that if ϕ_1 leaks into the input port, it does not produce a signal within the baseband signal at the output.

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These signals can, in general, be random, pseudo-random, periodic functions of time, analogue or digital waveforms.

It would be clear to one skilled in the art that virtual LO signals may be generated which provide the benefits of the invention to greater or lesser degrees.

- 5 While it is possible in certain circumstances to have almost no LO leakage, it may be acceptable in other circumstances to incorporate virtual LO signals which still allow a degree of LO leakage.

Exemplary sets of acceptable waveforms are presented in **Figures 4(a) and 4(b)**, plotted in amplitude versus time. In **Figure 4(a)**, five cycles of the VLO signal are presented, labelled ϕ_1 ϕ_2 . It is important to note that at no point in the operation of the circuit is an actual " ϕ_1 ϕ_2 " signal ever generated; the mixers receive separate ϕ_1 and ϕ_2 signals, and mix them with the input signal using different physical components. Hence, there is no LO signal which may leak into the circuit. The states of these ϕ_1 and ϕ_2 signals with respect to the hypothetical ϕ_1 ϕ_2 output are as follows:

ϕ_1 ϕ_2	ϕ_1	ϕ_2
Cycle 1 - LO	HI	LO
Cycle 1 - HI	LO	LO
Cycle 2 - LO	HI	LO
Cycle 2 - HI	LO	LO
Cycle 3 - LO	LO	HI
Cycle 3 - HI	LO	LO
Cycle 4 - LO	HI	LO
Cycle 4 - HI	LO	LO
Cycle 5 - LO	LO	HI
Cycle 5 - HI	HI	HI

Similarly, **Figure 4(b)** presents a second exemplary set of acceptable waveforms, plotted in amplitude versus time. In this case, however, the waveforms

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repeat on a four cycle pattern. The states of these ϕ_1 and ϕ_2 signals with respect to the hypothetical $\phi_1 \phi_2$ output are as follows:

$\phi_1 \phi_2$	ϕ_1	ϕ_2
Cycle 1 - LO	LO	LO
Cycle 1 - HI	HI	LO
Cycle 2 - LO	LO	LO
Cycle 2 - HI	HI	LO
Cycle 3 - LO	HI	HI
Cycle 3 - HI	LO	HI
Cycle 4 - LO	HI	HI
Cycle 4 - HI	LO	HI

While these signals may be described as "aperiodic", groups of cycles may be repeated successively. For example, the pattern of the ϕ_1 and ϕ_2 input signals presented in **Figure 4(a)** which generate the $\phi_1 * \phi_2$ signal, repeat with every five cycles. Similarly, the pattern of the ϕ_1 and ϕ_2 input signals presented in **Figure 4(b)** repeat with every four cycles. Longer cycles could certainly be used.

It would be clear to one skilled in the art that many additional pairings of signals may also be generated. The more thoroughly the above criteria (i) - (vi) for selection of the ϕ_1 and ϕ_2 signals are complied with, the more effective the invention will be in overcoming the problems in the art.

As well, rather than employing two mixing signals shown above, sets of three or more may be used (additional description of this is given hereinafter with respect to **Figure 12**).

The topology of the invention is similar to that of two stage or multistage modulators and demodulators, but the use of irregular, time-varying mixer signal provides fundamental advantages over known transmitters and receivers. For example:

- minimal 1/f noise;
- minimal imaging problems;
- minimal leakage of a local oscillator (LO) signal into the RF output band;
- removes the necessity of having a second LO and various (often external) filters; and

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- has a higher level of integration as the components it does require are easily placed on an integrated circuit. For example, no large capacitors or sophisticated filters are required.

The invention provides the basis for fully integrated communications transmitters and receivers. Increasing levels of integration have been the driving impetus towards lower cost, higher volume, higher reliability and lower power consumer electronics since the inception of the integrated circuit. This invention will enable communications devices to follow the same integration route that other consumer electronic products have benefited from.

Specifically, advantages from the perspective of the manufacturer when incorporating the invention into a product include:

1. significant cost savings due to the decreased parts count of an integral device. Decreasing the parts count reduces the cost of inventory control, reduces the costs associated with warehousing components, and reduces the amount of manpower to deal with higher part counts;
2. significant cost savings due to the decreased manufacturing complexity. Reducing the complexity reduces time to market, cost of equipment to manufacture the product, cost of testing and correcting defects, and reduces time delays due to errors and problems on the assembly line;
3. reduces design costs due to the simplified architecture. The simplified architecture will shorten the first-pass design time and total design cycle time as a simplified design will reduce the number of design iterations required;
4. significant space savings and increased manufacturability due to the high integrability and resulting reduction in product form factor (physical size). This implies huge savings throughout the manufacturing process as smaller device footprints enable manufacturing of products with less material such as printed circuit substrate, smaller product casing, and smaller final product packaging;
5. simplification and integrability of the invention will yield products with higher reliability, greater yield, less complexity, higher life span and greater robustness; and
6. due to the aforementioned cost savings, the invention will enable the creation of products that would otherwise be economically unfeasible.

Hence, the invention provides the manufacturer with a significant competitive advantage.

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From the perspective of the consumer, the marketable advantages of the invention include:

- lower cost products, due to the lower cost of manufacturing;
- higher reliability as higher integration levels and lower parts counts imply products will be less prone to damage from shock, vibration and mechanical stress;
- higher integration levels and lower parts counts imply longer product life span;
- lower power requirements and therefore lower operating costs;
- higher integration levels and lower parts counts imply lighter weight and physically smaller products; and
- the creation of economical new products.

The invention can be applied in many ways which would be clear to one skilled in the art. A number of manners of creating VLO signals and applying them are described hereinafter, but it is understood that these embodiments are exemplary and not limiting.

Since the mixers in most transceivers act as solid state switches being turning on and off, it is preferable to drive the mixers using square waveforms rather than sinusoids. Square waveforms with steep leading and trailing edges will switch the state of the mixers more quickly, and at a more precise moment in time than sinusoid waveforms.

It is also important to note that in many modulation schemes, it is necessary to modulate or demodulate both in-phase (I) and quadrature (Q) components of the input signal, which requires a modulator or demodulator 90 as presented in the block diagram of **Figure 5**. In this case, four modulation functions would have to be generated: ϕ_{11} , which is 90 degrees out of phase with ϕ_{1Q} ; and ϕ_{21} which is 90 degrees out of phase with ϕ_{2Q} . The pairing of signals ϕ_{11} and ϕ_{21} must meet the function selection criteria listed above, as must the signal pairing of ϕ_{1Q} and ϕ_{2Q} . The mixers 92, 94, 96, 98 are standard mixers as known in the art.

As shown in **Figure 5**, mixer M1I 92 receives the input signal $x(t)$ and mixes it with ϕ_{11} ; subsequent to this, mixer M2I 94 mixes signal $x(t) \phi_{11}$ with ϕ_{21} to yield the in-phase component of the input signal, that is, $x(t) \phi_{11} \phi_{21}$. A complementary process occurs on the quadrature side of the demodulator, where mixer M1Q 96 receives the input signal $x(t)$ and mixes it with ϕ_{1Q} ; after which mixer M2Q 98 mixes signal $x(t) \phi_{1Q}$ with ϕ_{2Q} to yield the quadrature phase component of the input signal, that is, $x(t) \phi_{1Q}$

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ϕ_{20} . Several of the synthesizer 76, 78 designs presented herein produce in-phase components only, but it would be clear to one skilled in the art how to generate complementary quadrature mixing signal pairs. Generally, separate in-phase and quadrature channels have not been identified in the interests of simplicity.

Several methods of generating such VLO signals are presented in **Figures 6** through **10**. Since the LO-leakage problem can occur when power is generated at frequencies in the RF band anywhere on chip, it is preferable that condition (iv) stated above be followed for intermediate signals produced during the generation of the signals ϕ_1 and ϕ_2 . However, since the leakage path to these intermediate signals often provide some isolation, in such a case the condition on the intermediate signals can be somewhat relaxed.

The synthesizer **100** presented in **Figure 6** uses an input square wave (2LO) at twice the frequency of the RF carrier of the signal being modified by a signal denoted as S. Signal S could be the signal being modified, provided the criteria for the ϕ_1 and ϕ_2 signals are met, though generally it will be an independently generated control signal. This control signal S could also be generated using a delta-sigma (Δ - S) modulator which is known in the art.

A pulse swallower **102** is then used to remove pulses from the 2LO square wave. The pulse swallower **102** is controlled by the input signal S, such that when the input signal, S, switches state, a pulse is removed from the 2LO signal. The resulting signal is then passed through a divide-by-2 circuit **104** to produce the $\phi_1(t)$ output signal. The input signal S passes through a delay circuit **106** which delays it by the amount of time it takes the 2LO signal to propagate through to the $\phi_1(t)$ output, so that the two signals are synchronized. The output of this delay circuit **106** is the $\phi_2(t)$ mixer signal.

Assuming that the input signal S follows no regular pattern, the output signals $\phi_1(t)$ and $\phi_2(t)$ could be random or pseudo-random. Since this circuit uses an oscillator at twice the carrier frequency of the input signal, there is no LO signal to leak to the output or into other parts of the circuit. Similarly, none of the intermediate signals, nor either of the mixer signals ϕ_1 and ϕ_2 , has an LO frequency component.

A logic circuit that performs the function of **Figure 6** is presented in **Figure 7**. The pulse swallower **102** consists of a standard delay latch (D-latch) **D1**. A D-latch is a flip-flop whose input passes to the output after one clock cycle. The triggering of the pulse swallower **102** is controlled by D-latches **D4** through **D7** and the exclusive OR (XOR) gate **XOR1**, which detect the leading edge of the input signal S and

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create a pulse which causes **D1** to swallow a pulse of the input signal **2LO**.

D-latches **D2** and **D3** form a divide-by-two circuit **104** that receives the output of **D1** and produces the ϕ_1 mixing signal. The D-latches **D4** through **D7** also delay the **S** signal to produce the ϕ_2 signal. Note that this circuit produces both the I and Q

5 components of ϕ_1 and ϕ_2 , which would be required for input to a mixer such as that of **Figure 5**; subscripts indicate the signals required for the frequency translation of the in-phase and quadrature components of the input signal **S**, respectively.

Figure 8 presents another method for producing the signals ϕ_1 and ϕ_2 . Here, the D-latches **D8** through **D13** form a shift register which is clocked by the signal
10 **2LO**. The signal **2LO** is once again a square wave that has a frequency of twice the RF carrier frequency. The shift register can be initially loaded with a predetermined sequence and the output ϕ_1 will cycle through that sequence producing the desired output. The second output ϕ_2 is then produced by taking the output of consecutive taps from the shift register, and exclusive-ORing them together with gate **XOR2** to
15 produce a signal that can be used to clock a second shift register (**D14** and **D15**). The output of the second shift register is then ϕ_2 .

Figure 9 shows a method similar to that of **Figure 8**, except that signal ϕ_2 is generated by a second shift register (**D22** through **D27**), which is a duplicate of the shift register that produces the signal ϕ_1 (**D16** through **D21**). As well, there is a
20 difference in the initial loading of the shift registers; the first shift register being loaded with the sequence that will produce ϕ_1 , and the second being loaded with the sequence which will produce ϕ_2 .

The previous methods of generating ϕ_1 and ϕ_2 use an input signal at twice the RF carrier frequency (that is, **2LO**). In some situations it may be difficult to
25 design logic to operate at this frequency. If enough isolation can be obtained to protect an input of **LO** from leaking into the RF band, the method shown in **Figure 10** can be used.

Here the edges of the input signal **S** are aligned with the **LO** input edges through the D flip-flop **D28**. The inverter **I1** adds a delay to the **LO** input to make
30 sure the two signal edges remain aligned. The two signals are then passed through an exclusive OR (XOR) gate **XOR3** to produce the output signal ϕ_1 . Another delay is added to the output of the **D28** latch via inverter **I2** to keep the edges aligned with the output of the XOR gate **XOR3**. The output of **I2** is then ϕ_2 .

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The signal ϕ_2 can also be generated by using a shift register with feedback similar to those used in the generation of PN sequences for use in spread-spectrum communications. An example of such a shift register is shown in **Figure 11**. The D-latches **D29** through **D32** form a shift register which is clocked by the signal at twice the RF carrier frequency. **MOD1** does a modulo-2 multiplication of the output of **D31** with the output of **D32**, which is then fed into the input of **D32** to produce the required feedback. The signal ϕ_2 is then produced at the output of **D32**. A similar shift register with similar feedback can be used to produce the signal ϕ_1 . The conditions on the design of these shift registers are that they produce the signals ϕ_1 and ϕ_2 that have the properties mentioned above:

- $\phi_1(t) * \phi_2(t)$ must have a frequency component at the RF carrier frequency;
- $\phi_1(t) * \phi_2(t)$ must not contain a significant amount of power at frequencies other than the RF carrier frequency; and
- $\phi_1(t)$ and $\phi_2(t)$ must not contain a significant amount of energy in the RF signal bandwidth.

The signals of the invention may also be generated in many other ways, which would be clear from the teachings herein. For example, ϕ_1 could be generated using a control signal S to selectively divide a 2LO signal by either 2 or by 4. In this case, if the value of S is a digital "0" then the 2LO signal could be divided by 2, and if the value of S is a digital "1", the 2LO signal could be divided by 4. The function ϕ_2 can be derived from the control signal S in a similar manner, to generate a pair of time-varying signals which meet the criteria of the invention to the extent required by the application.

The invention allows one to fully integrate a RF transmitter on a single chip without using external filters, while furthermore, the RF transmitter can be used as a multi-standard transmitter.

The construction of the necessary logic to generate the mixing signals of the invention would be clear to one skilled in the art from the description herein. Such signals may be generated using basic logic gates, field programmable gate arrays (FPGA), read only memories (ROMs), micro-controllers or other devices known in the art. Though the figures herein imply the use of analogue components, all embodiments can be implemented in digital form.

It would be clear to one skilled in the art that many variations may be made to the designs presented herein, without departing from the spirit of the invention. One such variation to the basic structure in **Figure 3** is to add a filter between the two

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mixers 72 and 74 to remove unwanted signals that are transferred to the output port. This filter may be a low pass, high pass, or band pass filter depending on the transmitter requirements, and may be purely passive, or have active components.

5 In Figure 3, two mixer signals are used to perform the down-conversion or up-conversion of $x(t)$. It is also possible to use more than two signals to accomplish the same goal. The block diagram of Figure 12 presents such a variation, where several functions $\phi_1, \phi_2, \phi_3 \dots \phi_n$ are used to generate the virtual LO. Here, $\phi_1 * \phi_2 * \dots * \phi_n$ has a significant power level at the LO frequency being emulated, but each of the functions $\phi_1 \dots \phi_n$ contain an insignificant power level at LO. Each of these
10 methods of signal generation can be easily extended to produce more than two signals.

The electrical circuits of the invention may be described by computer software code in a simulation language, or hardware development language used to fabricate integrated circuits. This computer software code may be stored in a variety
15 of formats on various electronic memory media including computer diskettes, CD-ROM, Random Access Memory (RAM) and Read Only Memory (ROM). As well, electronic signals representing such computer software code may also be transmitted via a communication network.

Clearly, such computer software code may also be integrated with the code
20 of other programs, implemented as a core or subroutine by external program calls, or by other techniques known in the art.

The embodiments of the invention may be implemented on various families of integrated circuit technologies using digital signal processors (DSPs), microcontrollers, microprocessors, field programmable gate arrays (FPGAs), or
25 discrete components. Such implementations would be clear to one skilled in the art.

The invention may be applied to various communication protocols and formats including: amplitude modulation (AM), frequency modulation (FM), frequency shift keying (FSK), phase shift keying (PSK), cellular telephone systems including analogue and digital systems such as code division multiple access (CDMA), time
30 division multiple access (TDMA) and frequency division multiple access (FDMA).

The invention may be applied to such applications as wired communication systems include computer communication systems such as local area networks (LANs), point to point signalling, and wide area networks (WANs) such as the Internet, using electrical or optical fibre cable systems. As well, wireless
35 communication systems may include those for public broadcasting such as AM and

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- FM radio, and UHF and VHF television; or those for private communication such as cellular telephones, personal paging devices, wireless local loops, monitoring of homes by utility companies, cordless telephones including the digital cordless European telecommunication (DECT) standard, mobile radio systems, GSM and
- 5 AMPS cellular telephones, microwave backbone networks, interconnected appliances under the Bluetooth standard, and satellite communications.

While particular embodiments of the present invention have been shown and described, it is clear that changes and modifications may be made to such embodiments without departing from the true scope and spirit of the invention.

ART 34 AMDT

WHAT IS CLAIMED IS:

1. A synthesizer for generating signals to be input to successive mixers for modulating or demodulating an input signal $x(t)$, said synthesizer comprising:
a first signal generator for producing a first mixing signal ϕ_1 which varies irregularly over time; and
a second signal generator for producing a second mixing signal ϕ_2 which varies irregularly over time;
where $\phi_1 * \phi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither ϕ_1 nor ϕ_2 has significant power at the frequency of said local oscillator signal being emulated.
2. The synthesizer of claim 1, wherein signals used to generate ϕ_1 and ϕ_2 do not have a significant amount of power at the output frequency of said output signal $x(t)$ ϕ_1 ϕ_2 .
3. The synthesizer of claim 2, wherein $\phi_1 * \phi_1 * \phi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)$ ϕ_1 ϕ_2 .
4. The synthesizer of claim 3, wherein $\phi_2 * \phi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)$ ϕ_1 ϕ_2 .
5. The synthesizer of claim 4, wherein said first and second mixing signals ϕ_1 and ϕ_2 are generating using a single time base.
6. The synthesizer of claim 4, wherein said first and second mixing signals ϕ_1 and ϕ_2 are digital waveforms.
7. The synthesizer of claim 4, wherein said first and second mixing signals ϕ_1 and ϕ_2 are square waveforms.
8. The synthesizer of claim 4, wherein said first and second mixing signals ϕ_1 and ϕ_2 are randomly generated.
9. The synthesizer of claim 4, wherein said first and second mixing signals ϕ_1 and ϕ_2 are pseudo-randomly generated.

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10. The synthesizer of claim 4, wherein said first and second mixing signals ϕ_1 and ϕ_2 are periodic functions of time.
11. The synthesizer of claim 4, wherein said first and second signal generators comprise:
pulse removal means for removing pulses from a local oscillator signal which has a frequency of twice the RF carrier, generating said first mixing signal ϕ_1 ; and
complementary means for generating said second mixing signal ϕ_2 .
12. The synthesizer of claim 4, wherein said pulse removal means comprises:
a pulse swallower for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and swallowing each pulse with a control signal S; and
a divide by two circuit for receiving and dividing said pulse swallowed signal by two, producing said first mixing signal ϕ_1 .
13. The synthesizer of claim 12, wherein said complementary means comprises:
a delay circuit for receiving and delaying said control signal S to be synchronized in time with said first mixing signal ϕ_1 , outputting said delayed control signal S as said second mixing signal ϕ_2 .
14. The synthesizer of claim 4, wherein said first and second signal generators comprise:
shift register means for generating said first and second mixing signals ϕ_1 and ϕ_2 by shifting out corresponding predetermined sequences.
15. The synthesizer of claim 14, wherein said shift register means comprises:
a shift register for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said first mixing signal ϕ_1 , by shifting out a predetermined sequence.
16. The synthesizer of claim 15, wherein said second signal generator comprises:
an exclusive-OR (XOR) circuit for comparing outputs of consecutive latches in said shift register; and

a second shift register being clocked by said XOR output, and generating said second mixing signal ϕ_2 , by shifting out a second predetermined sequence.

17. The synthesizer of claim 15, wherein said second signal generator comprises:

a third shift register for receiving said oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said second mixing signal ϕ_2 , by shifting out a predetermined sequence.

18. The synthesizer of claim 4, wherein said first and second signal generators comprise:

means for generating said first mixing signal ϕ_1 from an oscillator signal at the frequency of the local oscillator signal being emulated, and a control signal S having edges aligned with said oscillator signal; and

means for delaying said control signal S to produce said second mixing signal ϕ_2 .

19. The synthesizer of claim 18, wherein said means for delaying comprises:

a delay latch for sampling said control signal S at the frequency of the local oscillator signal being emulated; and

an inverter for receiving and inverting said delay latched control signal S to produce said second mixing signal ϕ_2 .

20. The synthesizer of claim 19, wherein said means for generating said first mixing signal ϕ_1 comprises:

a second inverter for receiving the oscillator signal at the frequency of the local oscillator signal being emulated; and

an exclusive-OR (XOR) circuit for comparing said inverted oscillator signal with said latched input signal $x(t)$, producing said first mixing signal ϕ_1 .

21. The synthesizer of claim 4, wherein said first signal generator comprises:

a shift register with a feedback loop.

22. The synthesizer of claim 21, wherein said first signal generator comprises:
a shift register for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said first mixing signal ϕ_1 , by shifting out a predetermined sequence; and
a modulo-2 multiplier for receiving said first mixing signal ϕ_1 and the output of an earlier latch in said shift register, feeding an output into a later latch in said shift register.
23. The synthesizer of claim 4 comprising:
one or more additional signal generators for producing one or more additional mixing signals, varying irregularly over time;
where the product of all of said mixing signals has significant power at the frequency of a local oscillator signal being emulated, and none of said all of said mixing signals has significant power at the frequency of said local oscillator signal being emulated.
24. The synthesizer of claim 4, where said first signal generator comprises:
a divide by 2 circuit for receiving an oscillator signal at the frequency of the local oscillator signal being emulated; and
a divide by 4 circuit for receiving said oscillator signal at the frequency of the local oscillator signal being emulated;
selector means for routing either the output of said divide by 2 circuit or said divide by 4 circuit to an output, said output producing said first mixing signal ϕ_1 .
25. The synthesizer of any one of claims 12, 13, 18, 19 or 20, wherein said control signal S comprises a random signal.
26. The synthesizer of any one of claims 12, 13, 18, 19 or 20, wherein said control signal S comprises a pseudo-random signal.
27. The synthesizer of any one of claims 12, 13, 18, 19 or 20, wherein said control signal S comprises a periodic signal.
28. The synthesizer of any one of claims 12, 13, 18, 19 or 20, comprising:
a delta-sigma (Δ -S) modulator for generating said control signal S.

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29. The synthesizer of claim 4 comprising:
first and second latches which are clocked via a common clock, to align said first and second mixing signals φ_1 and φ_2 .
30. The synthesizer of claim 4, wherein the patterns of said first and second mixing signals φ_1 and φ_2 are different from one another.
31. An integrated circuit comprising the synthesizer of any one of claims 1 - 30.
32. A computer readable memory medium, storing computer software code in a hardware development language for fabrication of an integrated circuit comprising the synthesizer of any one of claims 1 - 30.
33. A computer data signal embodied in a output wave, said computer data signal comprising computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio transmitter of any one of claims 1 - 30.

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

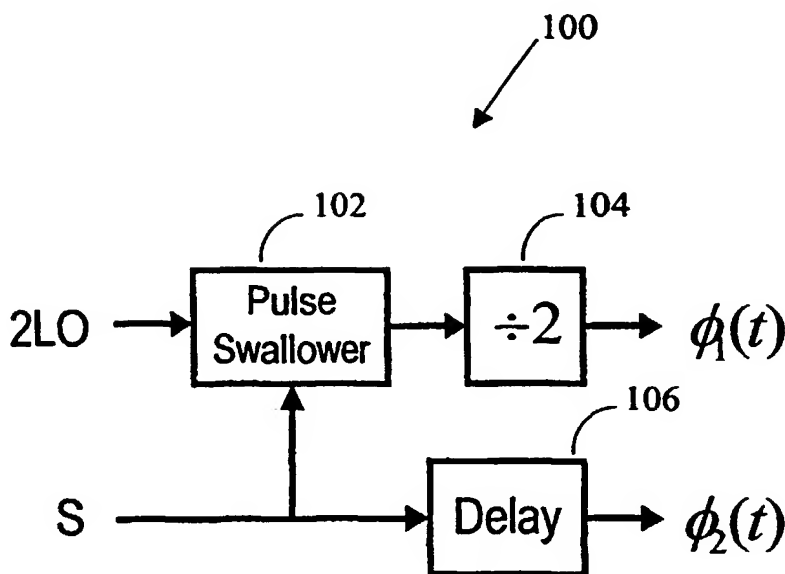
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(54) Title: IMPROVED METHOD AND APPARATUS FOR UP- AND DOWN-CONVERSION OF RADIO FREQUENCY (RF) SIGNALS



(57) Abstract: This patent describes a method and system which overcomes the LO-leakage problem of direct conversion and similar RF transmitters and receivers. To solve this problem a virtual LOTM signal is generated which emulates mixing with a local oscillator (LO) signal. However, the virtual local oscillator (VLO) signal is constructed using signals that do not contain a significant amount of power (or no power at all) at the wanted output RF frequency, so there is no LO component to leak to the output. The invention also does not require sophisticated filters or large capacitors as other designs in the art, so it is fully integratable.

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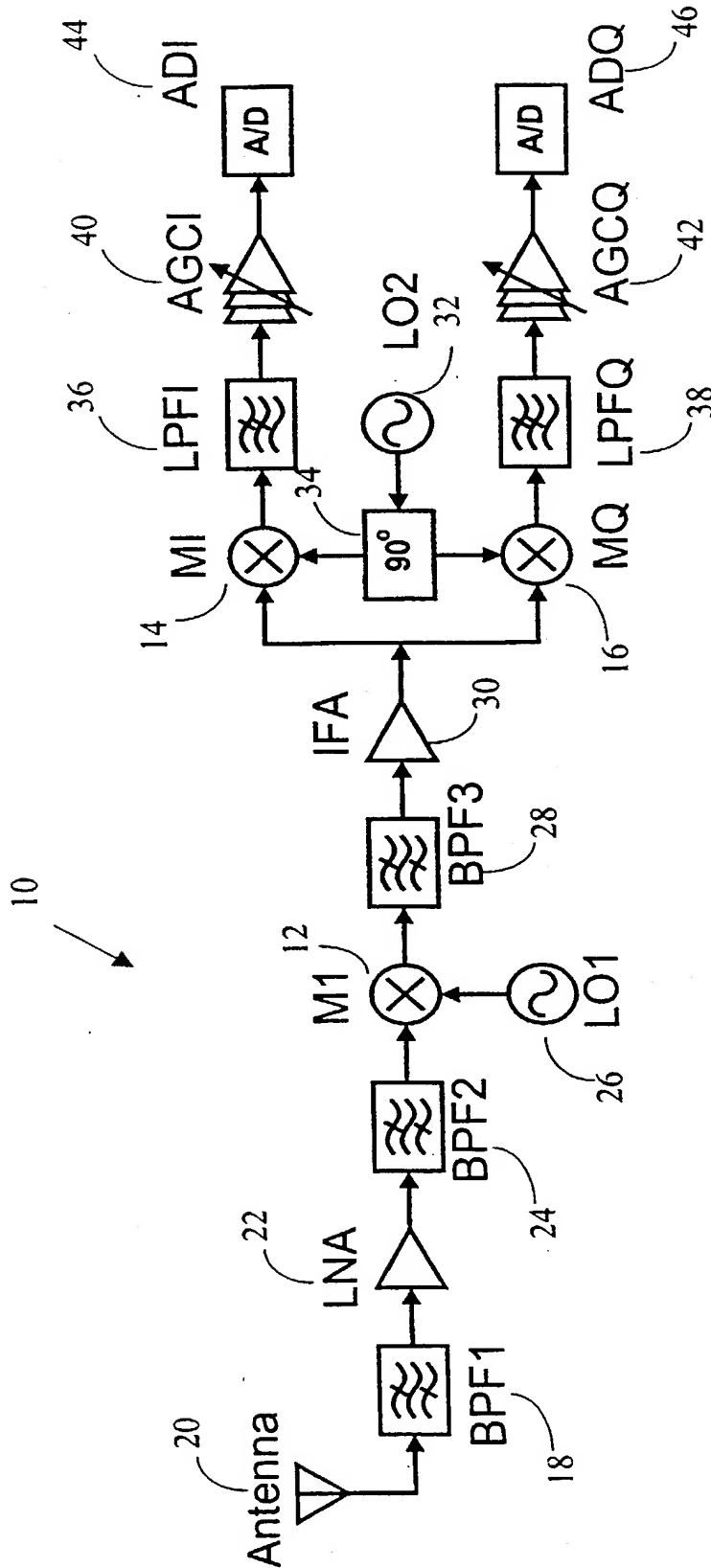


FIGURE 1 - PRIOR ART

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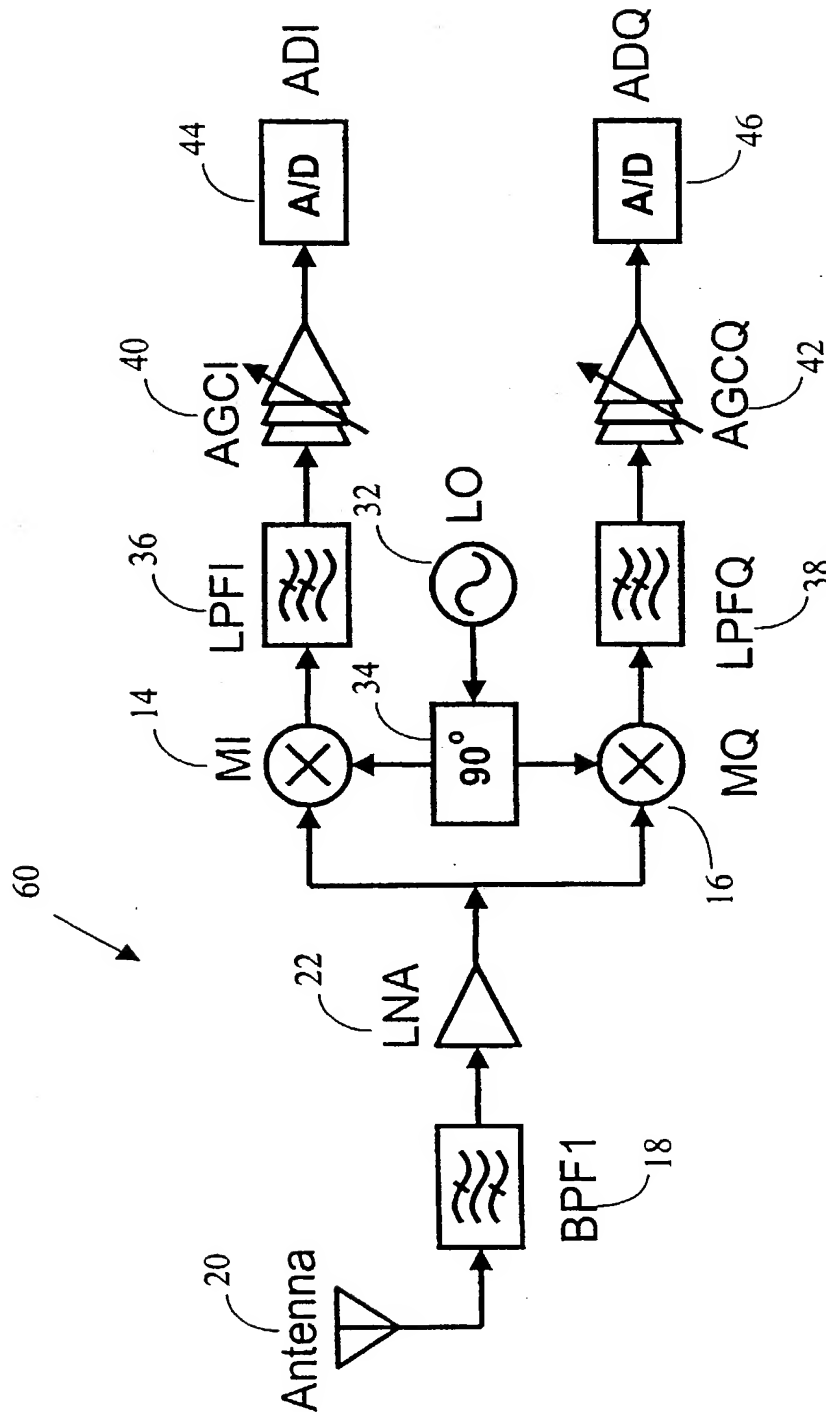


FIGURE 2 - PRIOR ART

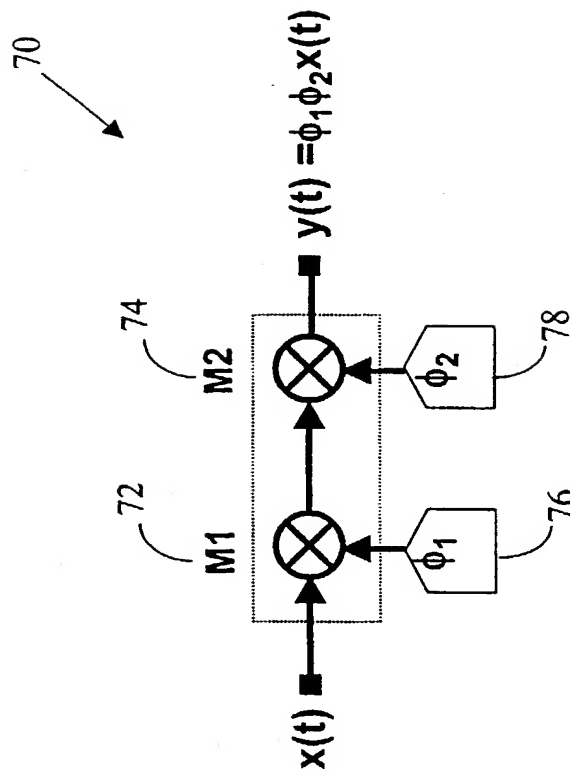
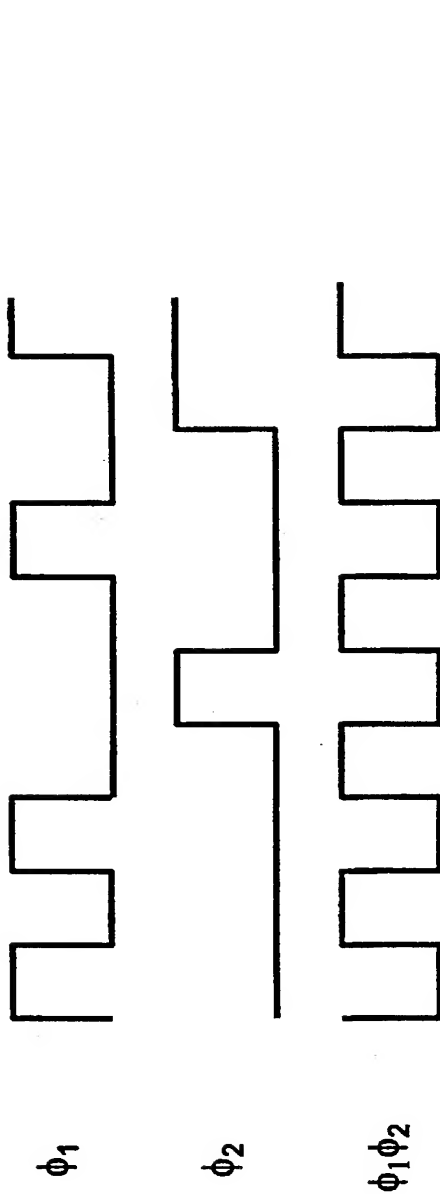
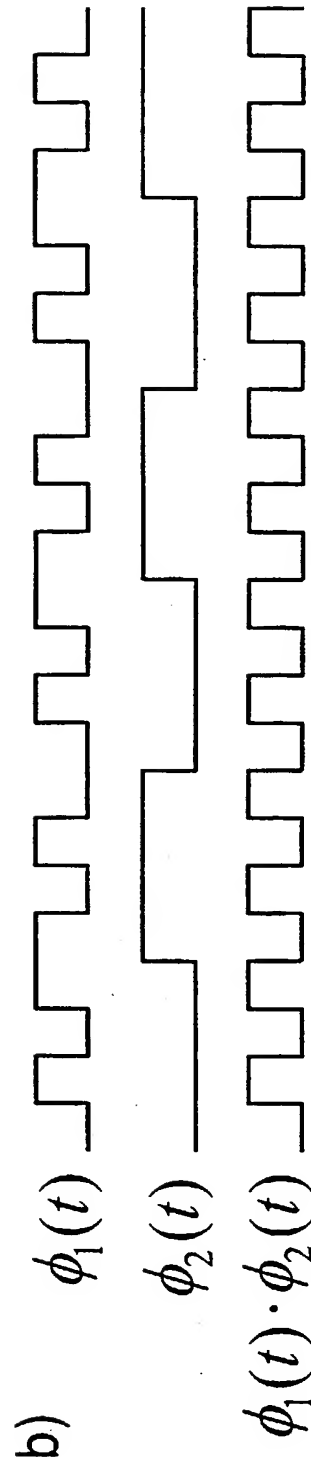


FIGURE 3

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a)



b)

FIGURE 4

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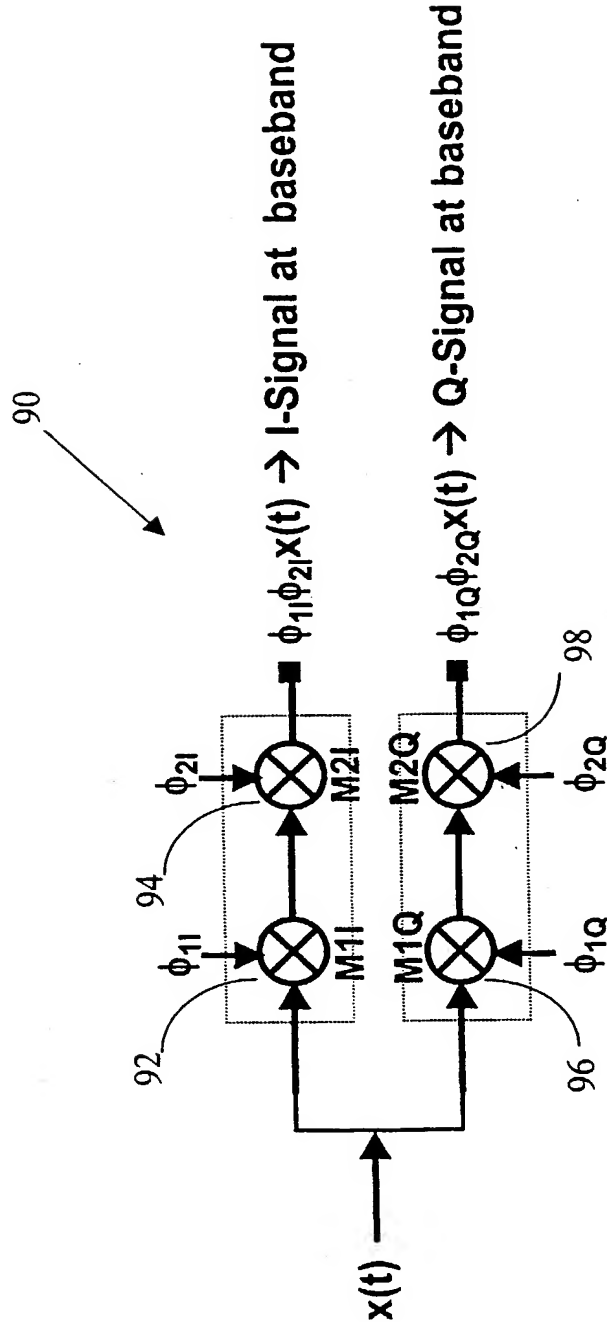


FIGURE 5

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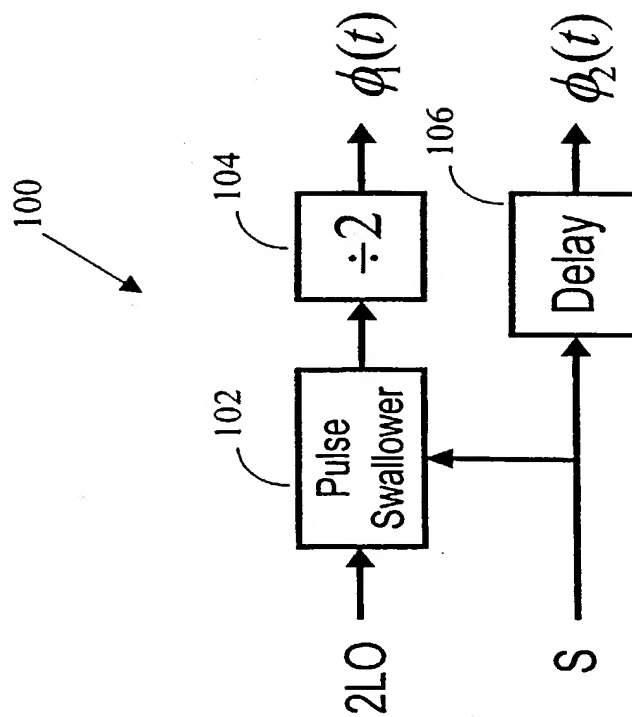


FIGURE 6

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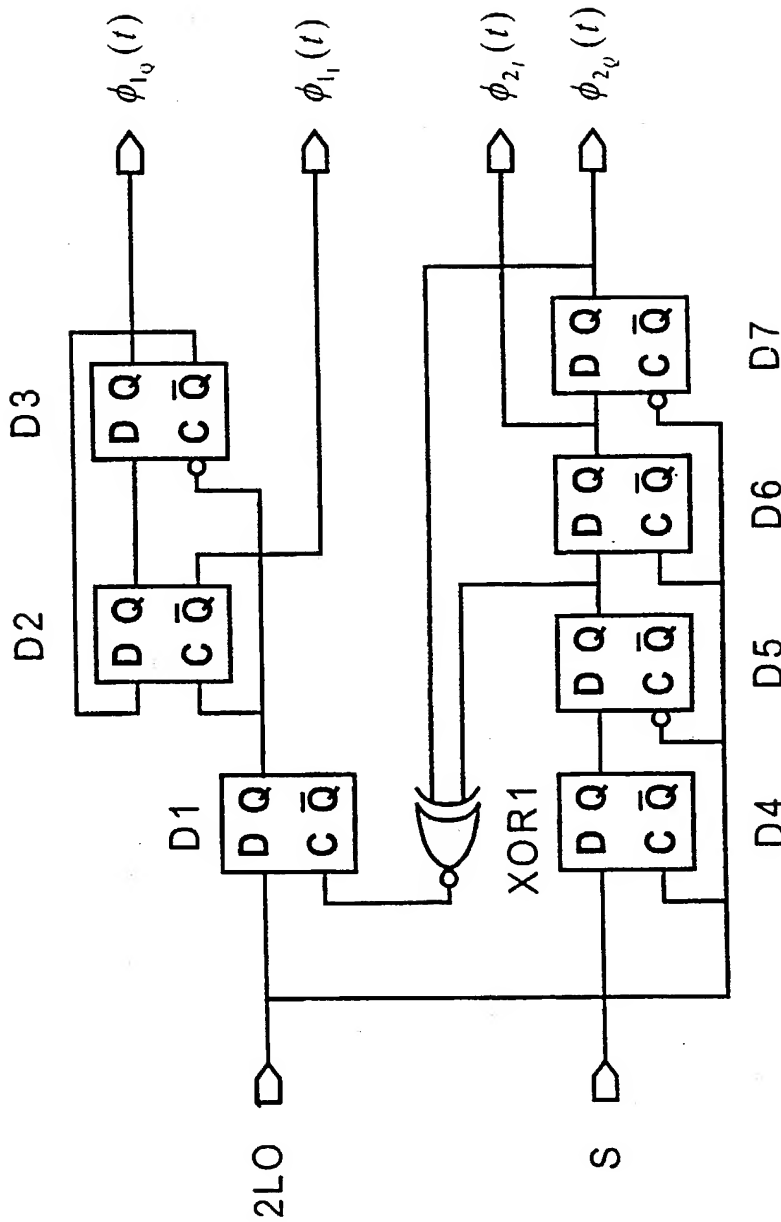


FIGURE 7

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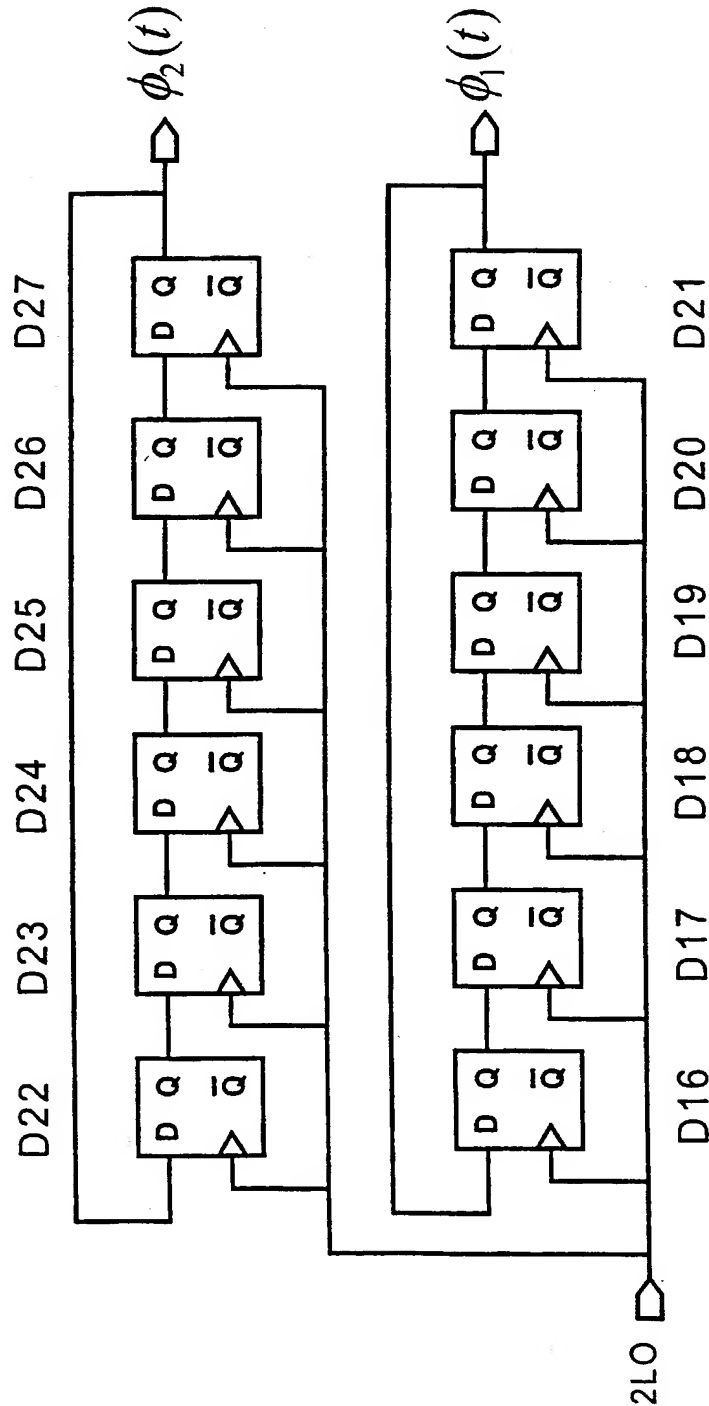


FIGURE 9

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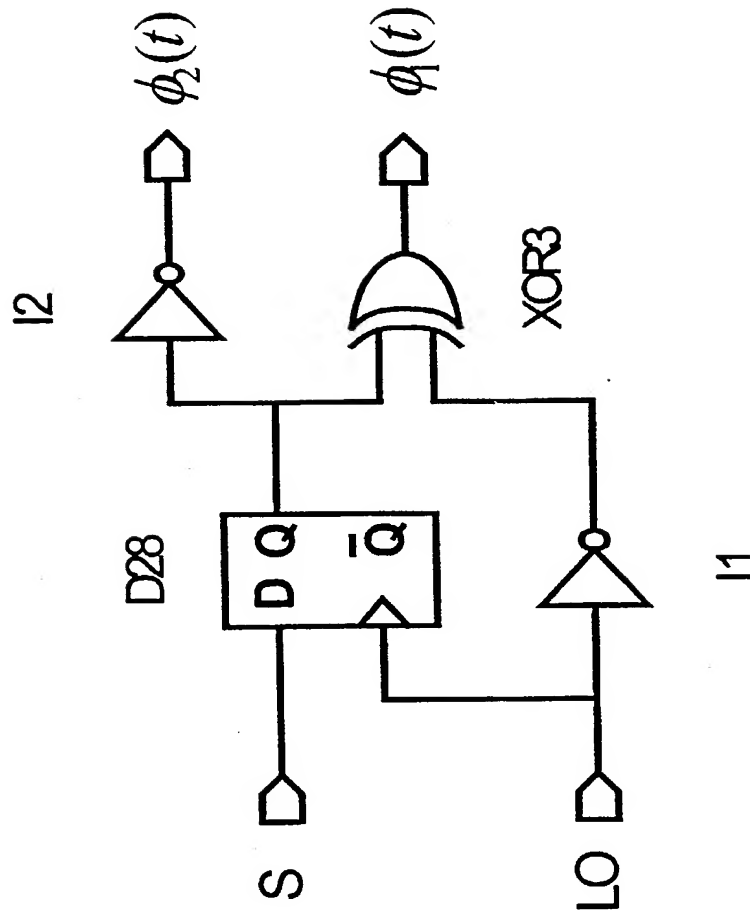


FIGURE 10

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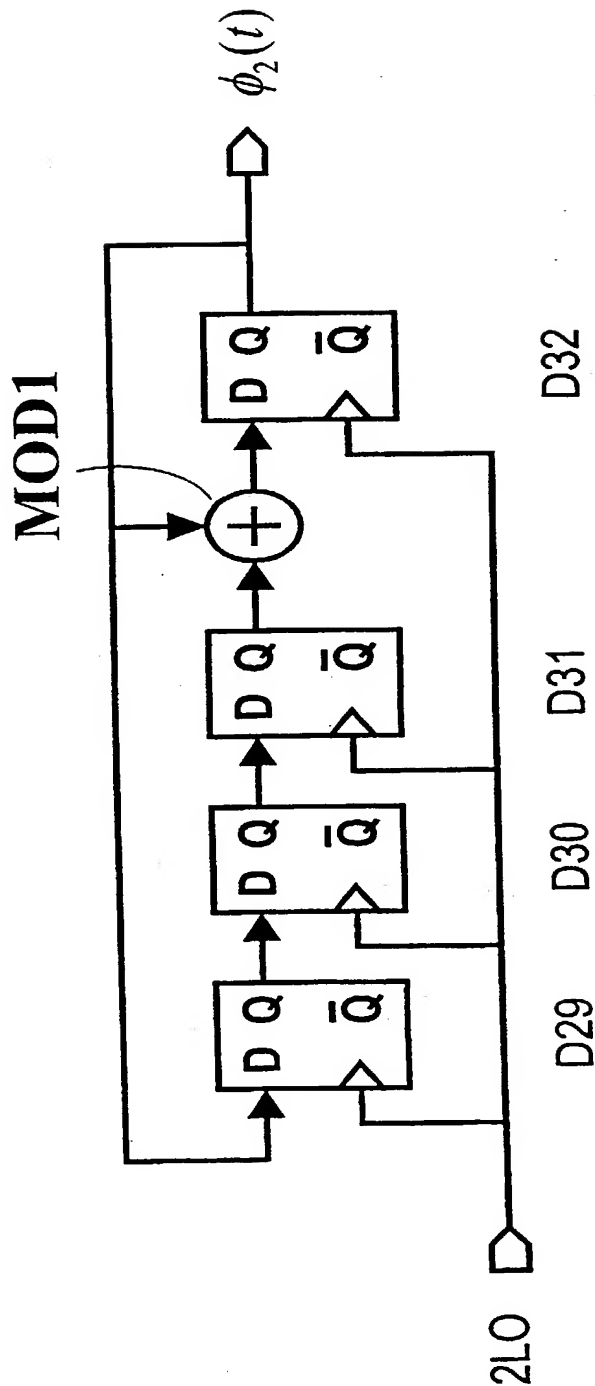


FIGURE 11

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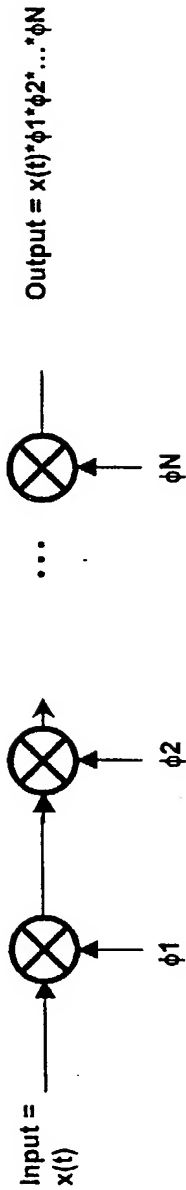


FIGURE 12

10 Rec'd PCT/PTO 29 JUL 2002 #4

Attorney Docket No. 085909-000000US

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **IMPROVED METHOD AND APPARATUS FOR UP-AND DOWN-CONVERSION OF RADIO FREQUENCY (RF) SIGNALS** the specification of which _____ is attached hereto or X was filed as U.S. Application No. 10/070,280 the National Phase of PCT/CA00/00996, filed September 1, 2000 and was amended on _____ (if applicable).

I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56. I claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Country	Application No.	Date of Filing	Priority Claimed Under 35 USC 119
Canada	2,281,236	September 1, 1999	Yes

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

Application No.	Filing Date

I claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application No.	Date of Filing	Status

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

The registered attorneys and agents associated with PTO Customer No. 20350

STATEMENT UNDER 37 CFR 3.73(b)Applicant/Patent Owner: Tajinder Manku et al.Application No./Patent No.: 10/070,280

Filed/Issue Date: _____

Entitled: IMPROVED METHOD AND APPARATUS FOR UP- AND DOWN-CONVERSION OF RADIO FREQUENCY
(RF SIGNALS)SIRIFIC WIRELESS CORPORATION, a Corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☒ the assignee of the entire right, title, and interest; or
2. ☐ an assignee of less than the entire right, title and interest.
The extent (by, percentage) of its ownership interest is _____ %

in the patent application/patent identified above by virtue of either:

- A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

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The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

June 26, 2002
Date

DAVID BRENNAN
Typed or printed name

[Signature]
Signature

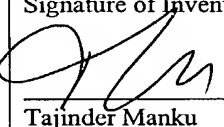
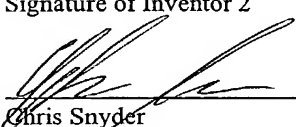


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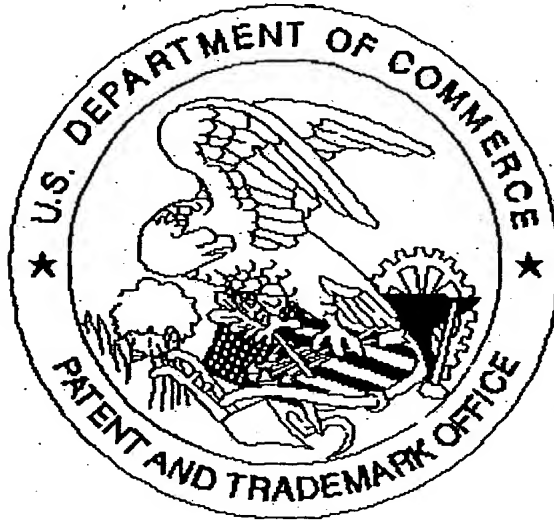
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I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor 1  Tajinder Manku Date: June 26/2002	Signature of Inventor 2  Chris Snyder Date: June 26, 2002
Signature of Inventor 3  Gareth Weale Date: 26/06/2002	Signature of Inventor 4  Lawrence Wong Date: June 26, 2002

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